AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~___~~") or placed in double brackets ("[[ ]]"), as applicable:

1. (Previously Presented) A method for realizing dynamic adjustment of data bandwidth in transmission equipment, comprising adding, by a device for realizing dynamic adjustment of data bandwidth in transmission equipment, a control channel in a trunk link of the transmission equipment for describing occupancy on time slots by a current service.

2. (Original) The method for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 1, wherein the control channel implements dynamic distribution on time slots in PCM line under control of CPU.

3. (Original) The method for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 2, wherein the dynamic distribution on time slots is controlled by channel control words written in the control channel, and the control channel comprises one or more time slots.

4. (Original) The method for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 1, wherein the current service comprises voice service and data service.

5. (Previously Presented) The method for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 1, wherein the method is applied in peer networking.

6. (Previously Presented) A device for realizing dynamic adjustment of data bandwidth in transmission equipment, comprising: a control word process circuit, a time slot distribution circuit and a CPU interface circuit, wherein the control word process circuit is designed to complete extraction and insertion of control information in control channel of E1/T1 link; the time slot distribution circuit is designed to complete separating voice time slots from Ethernet data time slots, and rebuilding data; the CPU interface circuit implements controlling on time slot distribution.

7. (Original) The device for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 6, wherein the device further comprises High Level Data Link Control (HDLC), Media Access Control (MAC) frame process circuit to implement processing HDLC link for Ethernet data, checking integrity of MAC frame, comparing and learning MAC addresses.

8. (Currently Amended) The device for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 6, wherein the time slot ~~dynamic~~ distribution circuit is controlled by channel control words written in a control channel, and the control channel comprises one or more time slots.

9. (Previously Presented) A method for realizing dynamic adjustment of data bandwidth in transmission equipment, comprising:

informing a time slot distribution circuit by CPU of time slots to be occupied by a voice service as voice call begins when a current service is multiplexed to a direction of E1/T1 link;

releasing the time slots from data service by the time slot distribution circuit; and distributing to the voice service;

informing the time slot distribution circuit by the CPU of the time slot having been released by the voice service after voice call finishes; and

distributing the time slots to Ethernet data service by the time slot distribution circuit, whereby dynamic adjustment of Ethernet data service is implemented.

10. (Previously Presented) The method for realizing dynamic adjustment of data bandwidth in transmission equipment of claim 1, wherein the device for realizing dynamic adjustment of data bandwidth in transmission equipment comprises: a control word process circuit, a time slot distribution circuit and a CPU interface circuit, the control word process circuit is designed to complete extraction and insertion of control information in the control channel of E1/T1 link; the time slot distribution circuit is designed to complete separating voice time slots from Ethernet data time slots, and rebuilding data; the CPU interface circuit implements controlling on time slot distribution.